# Lab Experiment 3

**Design of Finite State Machine (FSM) and Algorithmic State Machine**

**(ASM)**

**3.1 Objective:**

To learn the design of Finite State Machine (FSM) and Algorithmic State Machine (ASM) for any application in Verilog, simulating and synthesizing using EDA tools.

**3.2 Tools Required:**

1. Synthesis tool: Xilinx ISE
2. Simulation tool: Modelsim simulator

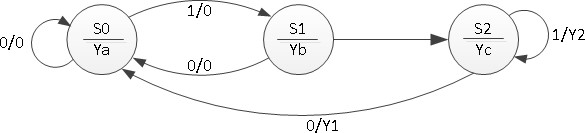
**3.3 Pre Lab Questions:**

1. Draw the simple model of FSM and ASM.
2. What is the basic Algorithm of Sequence Detector?
3. List the difference between Mealy and Moore Model.
4. What is ASM Chart and what are its main components?

**3.4 Problem:**

1. Implement Sequence recognizer for detecting three successive 1’s using Mealy Model (Behavioral Modeling).
2. Consider the following state graph of a sequential network which has both Mealy and Moore outputs. The outputs Y1 and Y2 are the Mealy outputs and so should be

conditional outputs. The Ya, Yb, and Yc are the Moore outputs so they should be part of state box. Input X can either be “0” or “1” and hence it should be part of the decision box.



Draw the ASM Chart for the above state graph and implement it using Verilog.

**3.5 Post lab Questions:**

1. Write Verilog code to implement an FSM using Moore Machine.